

# Void-Free Underfill Process With Variable Frequency Microwave for Higher Throughput in Large Flip Chip Package Application

Mamadou Diobet Diop, Marie-Claude Paquet, David Danovitch, and Dominique Drouin

**Abstract**—Moisture voiding in underfill materials can cause reliability issues for the flip chip packages. The bake-out step included in the assembly process flow to avoid this problem cannot be completely efficient for some large die size packages. This is due to complex substrate circuit designs and time delays subsequent to the bake-out step. This paper proposes using the variable frequency microwave cure to eliminate the moisture voiding of flip chip large packages assembled without any bake-out step. Results showed, for a given ramp rate, a decrease in voiding formation with decreasing VFM cure temperature. It was also found that, at low final cure temperatures, the hold steps promoted the voids formation more than the ramp steps. At high final cure temperatures, both ramp and hold steps induced voids formation, growth, and coalescence. Another interesting observation was that a slower ramp rate reduced void formation even at high cure temperature. Based on the voiding evolution study done here, two optimized cure profiles were proposed, one comprising a two-step approach and another using a one-step cure with a low ramp rate of 2 °C/min. These optimized VFM profiles demonstrated good adhesion and reliability results while providing a void-free underfill process without the need for a time-consuming bake-out step.

**Index Terms**—Flip chip, microwave, moisture, reliability, underfill voids.

## I. INTRODUCTION

**V**OIDING is one of the most prevalent underfill (UF) defects in flip chip plastic ball grid array (FCPBGA) application [1], [2]. Excessive sizes and/or levels of these voids can adversely impact the production yield by promoting defects

such as solder joint bridging and solder joint fatigue cracking [1], [3]–[5]. These defects are aggravated with the trend to larger die sizes, which are not only more prone to UF voiding [6] but are also more susceptible to thermal mismatch issues. As such, it becomes increasingly important to explore means to reduce or even eliminate UF voids.

The root causes of UF voiding are well documented and are typically divided into three categories [6]–[9]. First, moisture-related voids occur when moisture absorbed by the substrate composite layers (core + build-up + solder mask) outgases during the UF processing and becomes entrapped within the cured UF. A second void type is flow-related as a result of an uneven flow related to dispense method or material properties or solder joint design. Finally, UF voiding can be caused by flux-UF compatibility. This occurs when flux residues left after an improper cleaning or with a no-clean flux process react with the UF material, the reaction product can induce voids.

In the present work, we specifically focus on moisture-related voiding in the capillary UF process for large die size packages.

The traditional solution to prevent moisture-related UF voiding is to remove moisture absorbed by the substrate composite layers. This is done by performing a bake-out step at temperatures ranging from 125 °C to 150 °C prior to UF dispense [1]. The efficiency of the bake-out is of particular concern for high-end and large die flip chip packages due to the impact the substrate Cu loading design and density on the moisture diffusion mechanism. Several studies based on capacitance measurements and finite element modeling have shown that Cu circuitry and ground planes within the organic substrates act as moisture diffusion barriers. Hence, moisture may be trapped within the substrate composite layers during bake-out process, especially in the die region of the substrate where Cu loading is denser. This is corroborated by the works in [10], [11] which conclude a slower moisture desorption in substrate center, where the die was located, compared to edges. So, a complete moisture-free substrate would require tens of hours and, therefore, is not an acceptable solution for manufacturing [11], [12]. Another study by De Sousa *et al.* reveals the effect the number of build-up layers of the substrate on the rate of the moisture diffusion [7]. Indeed, the higher the number of build-up layers, the lower the moisture diffusion. Even in cases where the bake-out step is believed to have effectively eliminated moisture from the substrate, UF voiding has still been reported [13]. A possible explanation relates to the finding that the time delays between assembly steps

Manuscript received December 9, 2014; revised February 13, 2015; accepted February 19, 2015. Date of publication March 2, 2015; date of current version June 3, 2015. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada, by IBM Canada Ltd., by the MiQro Innovative Collaborative Centre (C2MI), and by Prompt Québec.

M. D. Diop was with the Computer and Electrical Engineering Department, Université de Sherbrooke, Sherbrooke, QC J1K 2R1, Canada. He is now with the Natural Sciences and Engineering Research Council of Canada/IBM Canada Industrial Research Chair in Smarter Microelectronics Packaging for Performance Scaling, Bromont, QC J2L 1A3, Canada (e-mail: diopdiobet@gmail.com).

M.-C. Paquet is with IBM Canada, Bromont, QC J2L 1A3, Canada (e-mail: mpaquet@ca.ibm.com).

D. Danovitch and D. Drouin are with the Computer and Electrical Engineering Department, Université de Sherbrooke, Sherbrooke, QC J1K 2R1, Canada (e-mail: David.Danovitch@USherbrooke.ca; Dominique.Drouin@USherbrooke.ca).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TDMR.2015.2408211

subsequent to the bake-out can have an influence on voiding. Indeed, moisture reabsorption of polymeric material used in the substrate composite layers should be taken into account. For example, it has been observed that the external layers above the Cu planes have higher moisture diffusion rates than the inner layers of the substrate due to smaller distance to travel to exit the substrate [11]. This promotes rapid reabsorption potential in the external layers of the substrates. Alternatively, the solder mask material, if insufficiently cured, is sensitive to moisture uptake that can cause void issues in the UF material [14], [15]. Therefore, the moisture sensitivity of any flip chip package will depend on its design and manufacturing steps. This makes it difficult to predict the acceptable moisture content for a void-free process of a given package. However, comparing weight measurements of substrates with UF void formation can be used to determine the acceptable moisture content of a package type [7].

We propose focusing on the curing method and profile in order to eliminate UF voiding. This was reached by curing the UF with the variable frequency microwave (VFM) oven. In flip chip application, the VFM-UF cure is essentially dedicated to package warpage reduction [16]–[18]. The UF void-free study presented here was done with a reduced assembly cycle time since the bake-out step was eliminated.

In Section II that follows, we review the experimental conditions to achieve these objectives. Samples and their moisture conditioning are first described. Then, the cure methods were detailed with a particular interest for the VFM cure. The measurement techniques to evaluate the voiding responses as well as the adhesion and reliability tests were presented. Section III reports on the results and discussions by analyzing the effect of the VFM profile variables on UF voiding. Optimized VFM profiles that lead to void-free processes with the no-bake packages are proposed. Finally, the preliminary qualification of the optimized VFM profiles will be covered with a particular emphasis on the failure mechanism observed in packages over the course of the reliability tests.

## II. MATERIALS AND METHODS

### A. Samples and Conditioning

The experiments were carried out with a flip chip package typical of those with a higher sensitivity to UF voiding. These packages comprised a large die ( $19.7 \times 19.7 \text{ mm}^2$ ), an organic substrate ( $42.5 \times 42.5 \text{ mm}^2$ ) and an experimental UF. The packages were assembled using a typical flip chip process. Additionally, a conditioning step of 2 hours at  $30 \text{ }^\circ\text{C}/60\%$  relative humidity (RH) was inserted between the bake-out and the UF dispense steps. Fig. 1 shows the process flow including the moisture conditioning step. The purpose of this conditioning was to create a high moisture level that will result in a reproducible void formation with a limited number of packages. The moisture level derived from such conditioning was considered to be much higher than that experienced in a typical factory ambient with or without a moisture bake-out step. Thus, it would be expected that any VFM profile that eliminates voids with moisture conditioned packages would

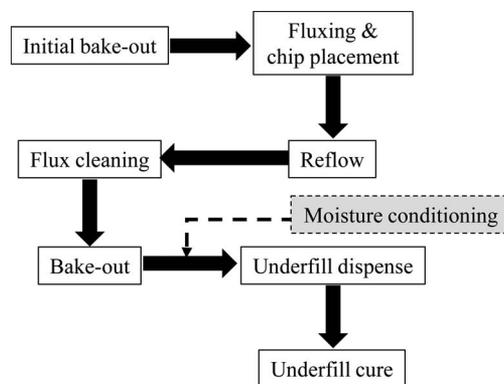


Fig. 1. Typical flip chip process flow with the moisture conditioning.

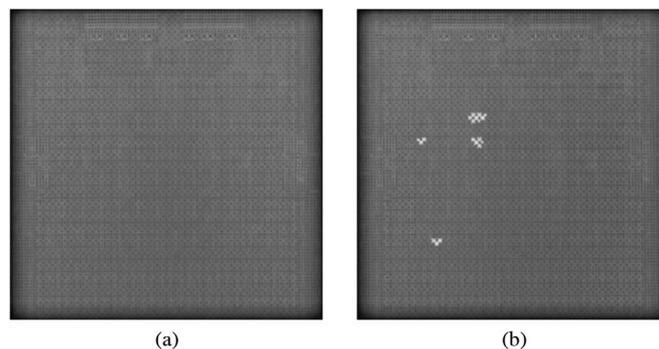


Fig. 2. C-SAM images of (a) non-conditioned package and (b) conditioned package (2 hrs– $30 \text{ }^\circ\text{C}/60\%$  RH) after a convection cure of  $165 \text{ }^\circ\text{C}/120 \text{ min}$ .

certainly result in void elimination with packages assembled without bake-out step. The effectiveness of moisture formation with the conditioning step is illustrated in Fig. 2. All these packages were cured by convection with the same profile of  $165 \text{ }^\circ\text{C}/120 \text{ min}$ . The parts with no voids (Fig. 2(a)) were not conditioned while the parts with voids (Fig. 2(b)) were moisture conditioned (2 hours at  $30 \text{ }^\circ\text{C}/60\%$  RH). Repeatable results were seen with a sample of six packages for each cure profile studied in Section III-A, III-B, and III-C. For the reliability tests in Section III-D, twelve packages were employed for each profile in order to cover the selected readouts.

### B. Cure Methods

The actual flip chip assembly process utilizes the standard convection method to cure the UF material. The UF convection curing is based on a flow of hot air which is transferred to the target packages, the oven walls and the fixtures. For the UF selected in this study, the typical convection cure profile comprised a ramp of  $5 \text{ }^\circ\text{C}/\text{min}$  up to  $165 \text{ }^\circ\text{C}$ , a hold at  $165 \text{ }^\circ\text{C}$  for 120 min then a ramp down to room temperature.

The VFM-UF cure was carried-out using a Microcure 3100 system from Lambda Technologies. The VFM oven is designed to avert hot spots or metal arcing during UF processing owing to a very fast cycling of more than four-thousand frequencies ranging from 5.8 to 7.0 GHz. An IR pyrometer was used to control the curing temperature through a closed-loop feedback system [18]. For the UF cure application, the VFM cure claims many advantages over the conventional convection approach.

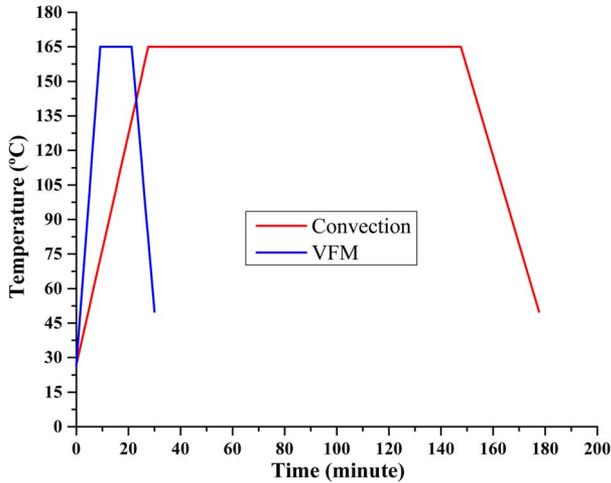


Fig. 3. Convection and VFM cycles comparison.

TABLE I  
VFM CURE PROFILES WITH EQUIVALENT CURING RATE VALUES

VFM profiles	Curing rate (%)
165 °C-12 min	96.0
145 °C-30 min	97.1
125 °C-55 min	98
100 °C-140 min	97.4
Convection 165 °C-120 min	95

Essentially, the VFM heating is selective since only the UF and the doped Si die are heated by the microwave energy whereas the organic substrate and the cavity air are not directly heated [17]. However, heat generated in the UF-die system can be transferred by conduction to the substrate by means of the dense Cu loading used in high-end packages [16]. VFM heats absorbing polymers faster than convection resulting in faster processing times. For instance, at the same convection cure temperatures, VFM is usually seen to reach a full cure of the UF with only 10% of the recommended convection time [16]. Also, VFM demonstrates a full cure of the UF at lower temperatures within times similar to that of convection cure [16]. These advantages are explained by the ability of the microwave energy to allow higher energetic molecular motions at the UF dipolar groups (O – H, N – H, C = O, ...) [17]. To exploit this capability, various VFM cure profiles were developed by testing several time-temperature combinations and varying the ramp rate values, while never exceeding the total convection cure cycle recommended for the current UF, i.e., 180 min. Fig. 3 compares cure cycles of the convection and the VFM methods to obtain an equivalent resultant degree of cure for the current UF. Degree of cure was measured using a DSC method where only fully VFM-cured UFs were selected for the voiding study. By convention, the UF cure was considered as complete when the degree of cure was equal to or exceeded 95%. Table I summarizes the degree of cure values for the selected VFM profiles and the standard convection cure.

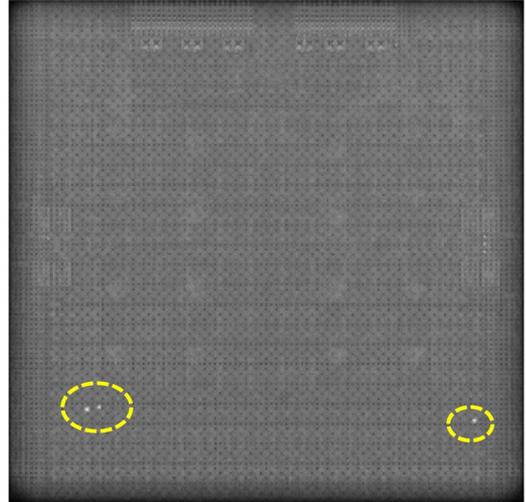


Fig. 4. High resolution CSAM image showing small voids of tens of microns.

### C. Voids Inspection Method

After the VFM cure, C-mode scanning acoustic microscopy (C-SAM) was employed to inspect the voids within the cured UF. High resolution scans were chosen in order to observe voids as small as tens of microns in size as illustrated in Fig. 4. To quantify individual and cumulative void areas, the C-SAM images were processed using the image processing and analysis software ImageJ 1.48 v.

### D. Adhesion and Reliability Tests

Some VFM cure profiles among those that provided void-free UF with packages assembled without bake-out steps were selected for a preliminary qualification. This consists of adhesion and reliability testing. The adhesion tests were performed by extracting the critical strain energy release rate,  $G_{IC}$ , from a modified cantilever beam approach detailed in [19] and presented in Fig. 5. These tests were conducted on parts for assessing the interfacial adhesion between the current UF and two common die passivation layers of silicon nitride ( $Si_3N_4$ ) and photosensitive polyimide (PSPI). All these parts were cured by both convection and VFM methods. Reliability was evaluated by deep thermal cycling (DTC) tests where packages were subjected to temperature cycles ranging from  $-55\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$ . Prior to performing these tests, the packages were submitted to lid attach step and a JEDEC preconditioning Level 3 ( $30\text{ }^\circ\text{C}/60\% \text{ RH}/192 \text{ hrs}$ ) with 3X reflow at  $260\text{ }^\circ\text{C}$ . Readouts for inspecting the mechanical integrity of the tested packages were conducted after 500, 1000, and 1500 cycles. There were two types of inspections including UF fillet observations for detecting any cracking and C-SAM scans for revealing any delamination around the die/UF interface.

## III. RESULTS AND DISCUSSION

### A. UF Voiding Evolution With VFM Profiles

This study was done at the VFM profiles of  $165\text{ }^\circ\text{C}$ -12 min,  $145\text{ }^\circ\text{C}$ -30 min,  $125\text{ }^\circ\text{C}$ -55 min, and  $100\text{ }^\circ\text{C}$ -140 min with

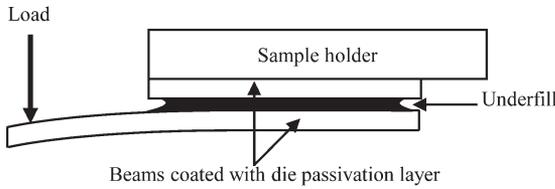


Fig. 5. Schematic of a modified cantilever beam adhesion test [18].

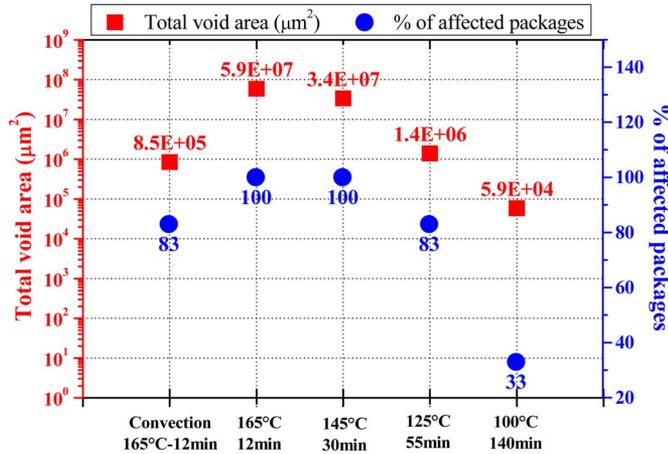


Fig. 6. Total void area and % of affected packages for the convection cure and the VFM profiles. All VFM profiles used a ramp rate of 15 °C/min.

the same ramp rate of 15 °C/min. Additionally, the convection cure of 165 °C-120 min at 5 °C/min ramp rate was done as a baseline test. Fig. 6 presents results for each profile in the form of a percent of packages inflicted with voids and an average void area per package. The C-SAM images of some void-affected packages are illustrated in Fig. 7 where the image #1 corresponds to the convection cure and the images #2 to #5 are related to the full VFM cures. For the VFM cure, the results show a decreasing trend in void area and number of affected packages when the cure temperature was lowered. The profile of 165 °C-12 min showed a surprisingly high amount of voids since almost all of the die area was covered by voids (Fig. 7-image#2). To a lesser extent, the 145 °C-30 min profile also induced a significant amount of voiding. Conversely, the profiles of 125 °C-55 min and the 100 °C-140 min displayed moderate and low voiding respectively. For the convection cure, voiding results were similar to the VFM cure at 125 °C-55 min.

A better understanding of this voiding evolution during VFM cure was obtained by discriminating the effect of the ramp and the hold steps. Basically, the full VFM cure test results of Fig. 6 were compared to partial VFM cure tests. This partial cure comprised a ramp of 15 °C/min up to the final cure temperature followed by a fast ramp down since the cured packages were exposed to room temperature after the VFM power shut-off. Images #6 to #8 of Fig. 7 show the partial cure results. The merged observations of the partial and full VFM cures produces the relationship depicted in Fig. 8 and thus provides greater insight into the evolution of the UF voiding within the VFM profile steps. Specifically, we derived that the hold step caused limited void formation at cure temperatures

less than 125 °C. The hold step, at cure temperatures greater than 145 °C, strongly encouraged void formation, growth and even coalescence. The ramp step can lead to void-free condition when the cure temperature was less than 125 °C. A significant void formation and growth was noticed during the ramp step at a temperature greater than 125 °C with additional coalescence when the temperature exceeded 145 °C. This tendency to greater voiding at higher VFM temperatures can be explained by considering the dipolar polarization mechanism. In fact, the electrical field of microwaves induces higher molecular collisions of the polar groups within the moisture contained in the substrate composite layers leading to dielectric heating [20]. As such, an increase in temperature will produce a higher molecular motions yielding an increase in moisture outgassing and transport. This means a higher propensity for the moisture to escape the confines of the substrate region and extend to the UF region.

### B. VFM Ramp Rate Effect on UF Voiding

The ramp rate is another parameter of the VFM profiles that must be considered. The effect of the ramp rate was studied by performing VFM partial cures up to 145 °C using different ramp rate values of 120 °C/min, 60 °C/min, 15 °C/min, 5 °C/min, and 2 °C/min. The percent of void-affected packages was extracted then presented in Table II. Lower ramp rates displayed greater robustness to voiding to the extent that no voids were seen with the ramp rate of 2 °C/min. Lower ramp rates corresponded to lower applied microwave energy and therefore the microwave electrical field acting on moisture polar groups was minimized. This is corroborated by the relationship between microwave power absorbed,  $P_{abs}$ , by a material at the temperature,  $T$ , during time,  $t$  [20]:

$$P_{abs} = \rho c_p \frac{\Delta T}{\Delta t} \tag{1}$$

Where,  $\rho$  and  $c_p$  refer to the mass, the density and the specific heat of the material.

Additionally, the UF was observed to begin hardening or crosslinking at lower ramp rates due to longer exposure times to VFM energy. This may act as a diffusion barrier to the outgassing moisture from the substrate, thereby inhibiting the void formation that could subsequently occur at the high VFM temperatures.

### C. VFM Profiles for Void-Free Processes

From a production manufacturing standpoint, it is important to discriminate voids regarding their size and dependent upon the solder joint pitch of a particular application. Larger voids are known to impact package integrity and smaller voids are benign in that the latter may be impossible to completely avoid when striving for a “void-free” UF process. The current study considered small voids as acceptable when they could not occupy the entire space between two adjacent solder joints of the current package. This averts a potential solder extrusion in a void during subsequent thermal processing that can lead to electrical shorting of adjacent solder joints. Nevertheless,

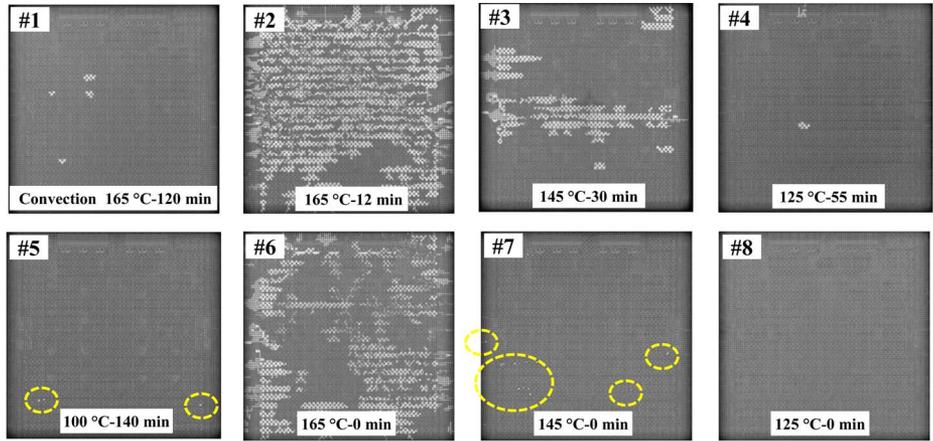


Fig. 7. C-SAM images of conditioned packages after a convection cure (#1), full VFM cures (#2–#5) and partial VFM cures (#6–#8). All VFM cures used a ramp rate of 15 °C-min.

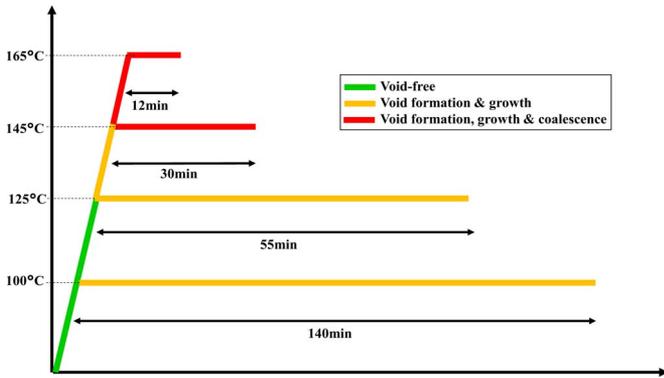


Fig. 8. Schematic of the UF voiding evolution with the VFM profile steps.

it is vital to identify the existence of such acceptable voids in the interest of future applications comprising finer pitch interconnections.

Based on the aforementioned results of profile experimentation, we proposed two VFM profile approaches to attaining a void-free condition. The first adopted a slow ramp rate of 2 °C/min up to different final cure temperatures of 165 °C, 145 °C, and 125 °C. The second approach corresponded to a two-step cure cycle of 85 °C-120 min +165 °C-12 min where each step was done with a ramp rate of 15 °C/min. The first hold step was chosen to initiate the crosslinking of the UF at the low temperature of 85 °C to prevent void formation while the second hold step at the high temperature of 165 °C completed the cure. The tests were performed with both the moisture conditioned packages and the no-bake-out packages. The voiding results for the aforementioned VFM profiles and the convection profile are presented in Table III. For the moisture conditioned packages, a very small amount of acceptable voids were seen with the two-step profile and the profile of 125 °C-55 min @2 °C/min. Void formation seems to take place during the hold step at 85 °C for the two-step profile and the hold at 125 °C-55 min for the 2 °C/min ramp rate. This confirms, on the one hand, the greater propensity to voiding during the hold step, even at 85 °C. On the other hand, we noted that the slow ramp rate of 2 °C/min was only effective in eliminating all

TABLE II  
RAMP RATE EFFECT ON VOID FORMATION AFTER A PARTIAL VFM CURE UP TO 145 °C

Ramp rate (°C/min)	120	60	15	5	2
% of affected packages	100	100	100	67	0

voids when the ramp step was sufficiently long. This induces UF hardening before the hold step take place, as demonstrated for the cases of 145 °C and 165 °C final cure temperatures.

Interestingly, all proposed VFM profiles provided a void-free process for the packages with no-bake-out step. This serves not only to support the potential to eliminating the bake-out step altogether, but also to further validate the margin of protection provided by using moisture conditioned packages in the development of an optimal UF cure process. Moreover, the proposed VFM profiles showed promising results over the standard convection cure in the sense that the latter provided voids for both conditioned and no-bake-out packages as seen in Table III.

D. Adhesion and Reliability Tests

The optimized profiles of 145 °C-30 min @2 °C/min and 85 °C-120 min + 165 °C-12 min @15 °C/min were selected for the adhesion and the reliability tests. For the adhesion tests, these two VFM profiles were compared to the convection cure as seen in Table IV. For the convection cure,  $G_{IC}$  values greater than 200 J/m<sup>2</sup> and a cohesive fracture mode near the passivation interface have been previously correlated to reliable material interfaces [19]. Conversely,  $G_{IC}$  values below this threshold, or with an adhesive fracture mode, have been considered to pose a high potential risk of delamination at the UF/material interfaces during subsequent thermal processing of actual packages [19]. Table IV shows two adhesion results tendencies depending upon the passivation layers and the cure method. The adhesion was slightly better with the VFM cured parts for the PSPI passivation while the adhesion was comparable for both curing method with the Si<sub>3</sub>N<sub>4</sub> passivation. This can be explained by the low microwave absorption of nitrides such as Si<sub>3</sub>N<sub>4</sub> [21]. Conversely, polyimides show high coupling with microwaves

TABLE III  
VOID IMPROVEMENT OF MOISTURE CONDITIONED AND NO-BAKE-OUT PACKAGES

Profiles	Moisture conditioned packages		No-bake-out packages	
	Void %	Void type	Void %	Void type
Convection cure 165°C-120min@ 5°C/min	High	Unacceptable	Medium	Unacceptable
VMF cure 85°C-2h + 165C-12min @ 15°C/min	Very low	Acceptable	No void	
VMF cure 165°C-12min @ 2°C/min	No void			
VMF cure 145°C-30min @ 2°C/min	No void			
VMF cure 125°C-55min @ 2°C/min	Very low	Acceptable	No void	

TABLE IV  
ADHESION TEST RESULTS AT UF/PSPI AND UF/Si<sub>3</sub>N<sub>4</sub> INTERFACES

Cure profiles	G <sub>IC</sub> (J/m <sup>2</sup> )	
	PSPI	Si <sub>3</sub> N <sub>4</sub>
Convection cure 165°C-120min@ 5°C/min	371±23	281±57
VFM cure 145C-30min @ 2C/min	425±21	306±8
VFM cure 85C-2h + 165C-12min @ 15C/min	457±46	276±9

as reported in [22], [23]. So, if complete PSPI cure was not reached during the parts preparation, this passivation can be directly heated by microwaves during the UF cure. This can result in enhancing the chemical bonding across the interface between the UF and the PSPI. In addition, cohesive fracture modes were seen with the VMF cured parts providing an evidence of good adhesion results.

For the reliability tests, the optimized VFM profiles were applied to packages assembled without any bake-out step and then compared to packages subjected to standard processing including bake-out and the standard convection cure. Results of the reliability testing are summarized in Table V. These results show that, after 500 cycles, no failure was observed for both convection and VFM cure methods. After 1000 cycles, cracking at the corner of the UF fillet and delamination at the UF/die interface were only detected with the convection cured packages. After 1500 cycles, the two types of failure were seen for both convection and VFM cure methods. Figs. 9 and 10 present the images of the UF fillet corner cracking and the UF/die interface delamination, respectively, as they appeared in the various cure profiles and at different cycling stages. We noted an increase in the severity of the failure after 1500 cycles; for example, we observed an increase in both the number of die corners failed and the severity of the delamination (Fig. 10(b)). It is interesting to note that the failures were all located at the die corners where the highest thermomechanical stresses are located. A better indication of the failure mechanism seen here has been reported in [24] where the first failure such as die sidewall delamination occurs around the die corner. Then, as thermal cycling continued, the sidewall delamination grew radially away from the corner resulting in UF fillet crack and UF/die interface delamination. The failure detected after 1000 cycles with the convection cure was suspected to be

related to the geometrical configuration of the selected package. Specifically a large die relative to the substrate size, causes higher thermomechanical stresses at the die corners. This is supported in a previous work where a higher die to substrate size ratio was associated with a lower package fatigue life [25]. Paquet *et al.* also attributed an increase in die size to earlier die sidewall delamination [24]. Additionally, while Table V suggests a slight reliability improvement of VFM cured packages over the convection method, it would be difficult to characterize this difference as being significant. Indeed, the severity and the failures seen after 1500 cycles were comparable for the three cure profiles, therefore for both cure methods. A more clear difference was seen in the work of Diop *et al.* where, for the type of package and UF material tested, the VFM cured packages demonstrated a better mechanical reliability than the convection cured package due to a lower post cure storage modulus [16]. Nevertheless, the fact that the optimized VFM profiles proposed here did not impair reliability is of particular interest in that these profiles were carried out in the absence of a prior package bake-out. So, we demonstrated that **VFM can provide a UF void-free process with a faster assembly cycle time while maintaining a good reliability compared to conventional flip chip process with convection cure.**

#### IV. CONCLUSION

This work investigated the use of the VFM cure method to eliminate moisture-related voids in UF materials. The impact of the cure final temperature, the ramp and hold steps and the ramp rate value on the voiding evolution were studied. As a result, **optimized VFM cure profiles were determined. They appear to provide more robust solutions in eliminating UF voids than the convection cure method for a flip chip assembly without bake-out step. This offers an important opportunity to reduce the assembly process cycle time and cost. Also, the optimized VFM cure profiles can be an alternative solution for packages with high moisture uptake.** The successful completion of the primary qualification steps for the flip chip production suggest that the VFM profiles recommended from this study can meet the requirements of next generation flip chip packages. Finally, it is believed, based on the mechanisms observed, that **the current work can be extended to eliminate UF voids caused by the outgassing of low molecular weight constituents.**

TABLE V  
DTC RESULTS

Cells	500 cycles		1000 cycles		1500 cycles	
	UF fillet	UF/Die interface	UF fillet	UF/Die interface	UF fillet	UF/Die interface
Convection cure 165°C-120min@ 5°C/min			Cracking	Delamination		
VFM cure 145C-30min @ 2C/min	No cracking	No delamination	No cracking	No delamination	Cracking	Delamination
VFM cure 85C-2h + 165C-12min @ 15C/min						

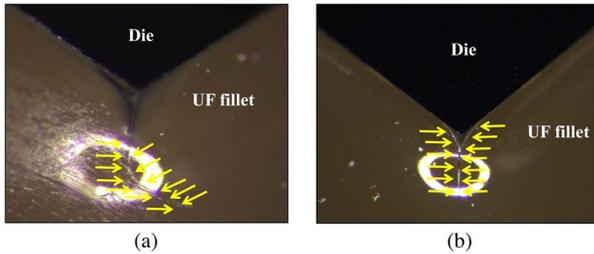


Fig. 9. Top views of the UF fillet corner cracks for two packages from the convection cure after (a) 1000 cycles and (b) 1500 cycles.

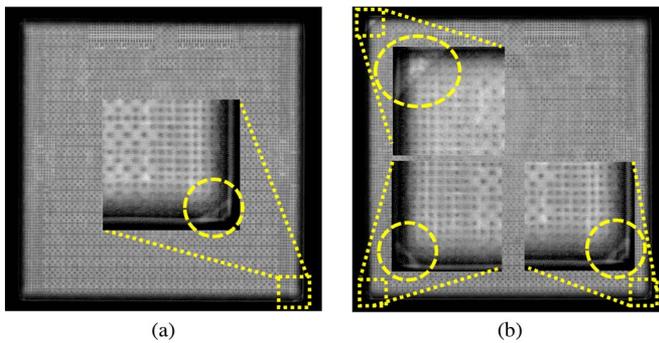


Fig. 10. C-SAM images of the UF/die delaminations for (a) a package from the VFM cure of 85 °C-2 h + 165 °C-12 min after 1000 cycles, (b) a package from the VFM cure of 145 °C-30 min after 1500 cycles.

## ACKNOWLEDGMENT

Authors would like to thank IBM's employees including Lise Brault for assistance with the experiments, Luc Bélanger and Thomas Lombardi for the packages and the IBM Bromont Canada chemistry laboratory team for the samples characterization. Also, special thanks are dedicated to Lambda Technologies employees for their technical support and valuable discussions.

## REFERENCES

- [1] K. J. Puttlitz and P. A. Totta, *Area Array Interconnection Handbook*. Norwell, MA, USA: Kluwer, 2001, pp. 480–481.
- [2] M. Klein, T. Murray, and T. Steen, "Laser ultrasonic inspection of flip chip underfill integrity," in *Proc. Int. Wafer Level Packag. Conf.*, San Jose, CA, USA, Oct. 10–12, 2004, pp. 1–3.
- [3] S. Lee and D. Baldwin, "Heterogeneous void nucleation study in flip chip assembly process using no-flow underfill," *J. Electron. Packag.*, vol. 136, no. 1, pp. 1–6, Dec. 2013.
- [4] T.-M. Niu, B. G. Sannakia, and S. Sathe, "Void-effect modeling of flip-chip encapsulation on ceramic substrate," *IEEE Trans. Compon. Packag. Technol.*, vol. 22, no. 4, pp. 484–487, Dec. 1999.
- [5] A. Genovese, F. Fontana, M. Cesana, S. Miliani, and P. Ermanno, "Solder extrusions and underfill delaminations: A remarkable flip chip qualification experience," *Int. J. Microcircuits Electron. Packag.*, vol. 24, no. 1, pp. 53–60, 2001.
- [6] P. S. Ho, Z. Xiong, and K. Chua, "Study on factors affecting underfill flow and underfill voids in a large-die flip chip ball grid array (FCBGA) package," in *Proc. 9th Electron. Packag. Technol. Conf.*, 2007, pp. 640–645.
- [7] I. De Sousa, L. Bélanger, C. Dufort, and S. DL Chénier, "A manufacturing approach to reducing underfill voiding on large die (> 18 mm)," in *Proc. Electron. Compon. Technol. Conf.*, 2011, pp. 1023–1029.
- [8] J. Wang, "The effect of flux residue and substrate wettability on underfill flow process in flip chip packages," in *Proc. Electron. Compon. Technol. Conf.*, 2006, pp. 467–473.
- [9] J. Libres and K. Robinson, "Challenges in the assembly of large die, high bump density Pb-free flip chip packages," in *Proc. Int. Electron. Manuf. Technol. Symp.*, 2007, pp. 346–351.
- [10] K. Weide-Zaage, W. Horaud, and H. Frémont, "Moisture diffusion in printed circuit boards: Measurements and finite-element-simulations," *Microelectron. Reliab.*, vol. 45, no. 9–11, pp. 1662–1667, Sep. 2005.
- [11] O. Thomas, C. Hunt, and M. Wickham, "Finite difference modelling of moisture diffusion in printed circuit boards with ground planes," *Microelectron. Reliab.*, vol. 52, no. 1, pp. 253–261, Jan. 2012.
- [12] N. Amin, A. Cheah, and I. Ahmad, "Effect of plasma cleaning process in the wettability of flip chip PBGA substrate of integrated circuit packages," *J. Appl. Sci.*, vol. 10, no. 9, pp. 772–776, May 2010.
- [13] Z. Kornain, A. Jalar, R. Rasid, and F. C. Seng, "Effect of curing profile to eliminate the voids/ black dots formation in underfill epoxy for Hi-CTE flip chip packaging," *World Acad. Sci., Eng. Technol.*, vol. 3, no. 35, pp. 909–914, Nov. 2009.
- [14] R. Zhao *et al.*, "Processing of fluxing underfills for flip chip-on-laminate assembly," in *Proc. APEX*, San Diego, CA, USA, 2002, pp. 1–18.
- [15] N.-C. Lee, *Reflow Soldering Processes and Troubleshooting SMT, BGA, CSP and Flip Chip Technologies*. Boston, MA, USA: Newnes, 2002, p. 231.
- [16] M. D. Diop, M.-C. Paquet, D. Drouin, and D. Danovitch, "Interactions between variable frequency microwave underfill processing and high performance packaging materials," in *Proc. 46th Int. Microelectron. Assembly Packag. Soc.*, Orlando, FL, USA., Sep. 30–Oct. 3, 2013, pp. 461–466.
- [17] R. L. Hubbard, Z. Pierino, and Z. Pukun, "Flip-chip process improvements for low warpage," in *Proc. Electron. Compon. Technol. Conf.*, 2010, pp. 25–30.
- [18] R. L. Hubbard and P. Zappella, "Low warpage flip-chip under-fill curing," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 12, pp. 1957–1964, Dec. 2011.
- [19] M.-C. Paquet *et al.*, "Underfill selection strategy for Pb-free, low-K and fine pitch organic flip chip applications," in *Proc. 56th Electron. Compon. Technol. Conf.*, 2006, pp. 1595–1603.
- [20] M. Gupta and E. W. W. Leong, *Microwaves and Metals*. Singapore: Wiley, 2007, p. 35.
- [21] Y. V. Bykov, K. I. Rybakov, and V. E. Semenov, "High-temperature microwave processing of materials," *J. Phys. D, Appl. Phys.*, vol. 34, no. 23, pp. R55–R75, Dec. 2001.
- [22] K. D. Farnsworth, R. N. Manéballi, S. A. Bidstrup-Allen, and P. A. Kohl, "Variable frequency microwave curing of photosensitive polyimides," *IEEE Trans. Compon. Packag. Technol.*, vol. 24, no. 3, pp. 474–481, Sep. 2001.
- [23] H. Matsutani *et al.*, "Low temperature curing of polyimide precursors by variable frequency microwave," *J. Photopolym. Sci. Technol.*, vol. 18, no. 2, pp. 327–332, 2005.
- [24] M.-C. Paquet, J. Sylvestre, E. Gros, and N. Boyer, "Underfill delamination to chip sidewall in advanced flip chip packages," in *Proc. Electron. Compon. Technol. Conf.*, 2009, pp. 960–965.
- [25] G. Caswell and C. Tulkoff, "The effect of coating and potting on the reliability of QFN devices," in *Proc. SMTA Int. Conf.*, 2013, vol. 1, p. 41.



**Mamadou Diobet Diop** received the Ph.D. degree in microelectronics from the Ecole Nationale Supérieure des Mines de Saint-Etienne, Saint-Etienne, France, in 2009.

From 2009 to 2011, he worked as a Postdoctoral Fellow with the Université du Québec à Montréal, Montreal, QC, Canada, in material reliability subjects for a rapid prototyping platform for electronic systems. From 2012 to 2013, as a Postdoctoral Fellow with the Université de Sherbrooke, Sherbrooke, QC, Canada, he worked on improving underfill processes in flip chip application with IBM Bromont.

Since 2014, he has been a Research Assistant with the Natural Sciences and Engineering Research Council of Canada/IBM Canada Industrial Research Chair in Smarter Microelectronics Packaging for Performance Scaling, Bromont, QC. His current research interests include developing alternative processes, as well as implementing new materials for reliable high-end flip chip packages. He also contributes to students' trainings on state-of-the-art equipment and laboratories.

Dr. Diop was a recipient of the 2013 IEEE Transactions on Components, Packaging and Manufacturing Technology Best Paper Award in the Advanced Packaging Category with the paper titled "Evaluation of anisotropic conductive films based on vertical fibers for post-CMOS wafer-level packaging."



**Marie-Claude Paquet** received the Bachelor's degree in physics engineering from the Université Laval de Québec, Québec, QC, Canada, and the Master's degree in mechanical engineering from the École Polytechnique de Montréal, Montréal, QC.

She is an Advisory Engineer at IBM Canada, Bromont, QC. She joined IBM in 1995, and her field of expertise is on polymeric encapsulation processes of microelectronics components. She is the author of several international conference publications and the holder of six U.S. patents. For the past ten years, she

has been concentrating on the development of high-end flip chip packaging, specifically adhesion enhancement processes, lower package stress alternatives, and improved material solutions for manufacturing.



**David Danovitch** received the Bachelor's and master's degrees in metallurgical engineering from McGill University, Montréal, QC, Canada.

He is an Associate Professor at the Computer and Electrical Engineering Department, Université de Sherbrooke, Sherbrooke, QC, Canada, and the holder of the Natural Sciences and Engineering Research Council of Canada/IBM Canada Industrial Research Chair in Smarter Microelectronics Packaging for Performance Scaling. Previous to this appointment, he was a Senior Technical Staff Member at IBM

Canada Bromont, QC, within the IBM Microelectronics Division, having worked with IBM for 32 years in various aspects of semiconductor device packaging. He has authored numerous technical publications. He is the holder of 41 patents.

Dr. Danovitch sits on a number of national and international committees on microelectronics.



**Dominique Drouin** received the Bachelor's degree in electrical engineering and the Ph.D. degree in mechanical engineering from the Université de Sherbrooke, Sherbrooke, QC, Canada, in 1994 and 1998, respectively.

He is a Chairholder of the Natural Sciences and Engineering Research Council of Canada/IBM Industrial Research Chair CRSNG/IBM in Smarter Microelectronics Packaging for Performance Scaling and has been a Professor at the Electrical and Computer Engineering Department at the Université de

Sherbrooke, since 1999. He is a co-inventor of a new approach for the fabrication of nanoelectronics devices featuring performances never reached before that has been acknowledged by the industry as a technology breakthrough. He has developed an expertise in the fields of nanoelectronics (single electron transistor and memory, metal-insulator-metal capacitor, resistive RAM) and materials characterization (SEM, CL, EDX, XPS). He also cumulates six years of industrial experience as Vice-President of operations within a start-up company (Quantiscript), where he was appointed to the development on new microfabrication processes.